Abstract

A logic circuit with improved performance when operating at the limits of the transistor's bandwidth. In particular, a latch includes a clocked trans-admittance stage circuit for receiving a voltage and producing a current output, and an active load, such as a trans-impedance stage circuit, connected to receive as input the current output of the trans-admittance stage circuit and produce a voltage output. Two independent trans-admittance and trans-impedance stages may be combined as a single latch pair. One or more latch pairs may be arranged in series as a cascaded chain and connected to the output current of a clocked trans-admittance stage latch.